

**Serial No. 10/664,845**

**IN THE TITLE:**

The title has been amended herein. Pursuant to 37 C.F.R. §§ 1.121 and 1.125 (as amended to date), please enter the title as amended.

**~~IMAGE SENSOR PACKAGES AND METHODS OF FABRICATION~~**

IN THE SPECIFICATION:

Please amend paragraph number [0003] as follows:

[0003] In response to large-scale production requirements, various attempts have been made to simplify the construction of image sensor packaging. U.S. Pat. No. 6,351,027 to Giboney et al. and U.S. Pat. No. 6,285,064 to Foster, for instance, disclose wafer-level packaging formed by laying a solid sidewall piece or an adhesive matrix over a wafer having an array of sensor devices and covering it with one or more transparent top pieces. The wafer is then singulated to create discrete chip-scale packages. While these packaging techniques reduce material costs and assembly steps, they do not completely protect the semiconductor chips from the environment and may require complicated process steps for forming electrical connections to the sensor devices. U.S. Pat. No. 6,266,197 to Glenn et al. discloses a method for forming image sensor packages wherein an array of image sensors is wire bonded to a carrier substrate, and a molded window array is placed over the array of image sensors. The substrate and attached molded window array are then singulated to form a plurality of individual image sensor packages. The molded window array of Glenn et al., however, suffers from the fact that individual transparent windows must be formed ~~within~~ within, or later attached to the molded array, requiring additional assembly and alignment steps during fabrication. U.S. Pat. No. 5,811,799 to Wu discloses an image sensor package formed by attaching a plurality of preformed or glue walls to an array of printed wiring frames having image sensors thereon and sealing the walls with transparent material. The printed wiring frames are then diced to form discrete packages. Once again, this arrangement may require the attachment or formation of multiple components during fabrication and may increase the occurrence of process contamination.

Please amend paragraph number [0014] as follows:

[0014] FIG. 1A is a top view of a semiconductor wafer containing an array of image sensor ~~chips~~ chips;

Please amend paragraph number [0015] as follows:

[0015] FIG. 1B is a sectional side view taken along line 1B-1B in FIG. ~~1A~~, 1A;

Please amend paragraph number [0016] as follows:

[0016] FIG. 2 is a top view of a transparent cover having a pattern of adhesive material applied ~~thereto~~, thereto;

Please amend paragraph number [0017] as follows:

[0017] FIG. 3 is a top view of the semiconductor wafer in FIG. 1A having a pattern of adhesive material applied ~~thereto~~, thereto;

Please amend paragraph number [0018] as follows:

[0018] FIG. 4A is a sectional side view of adhesive material positioned between bond pads and an image sensitive area of an image sensor ~~chip~~, chip;

Please amend paragraph number [0019] as follows:

[0019] FIG. 4B is a sectional side view of adhesive material covering bond pads around an image sensitive area of an image sensor ~~chip~~, chip;

Please amend paragraph number [0020] as follows:

[0020] FIG. 5 is a schematic representation of a backgrinding ~~process~~, process;

Please amend paragraph number [0021] as follows:

[0020.1] FIG. 6A is a top view of a semiconductor wafer;

[0021] FIGS. 6A and 6B are FIG. 6B is a sectional side view showing a first stage of a wafer dicing operation. view taken along line 6B-6B in FIG. 6A;

Please amend paragraph number [0022] as follows:

[0022] FIGS. 7A and 7B are sectional side views showing an alternative first stage of the wafer dicing ~~operation.~~ operation;

Please amend paragraph number [0023] as follows:

[0023] FIG. 8 is a sectional side view showing a second stage of the wafer dicing ~~operation.~~ operation;

Please amend paragraph number [0024] as follows:

[0024] FIG. 9 is a sectional side view showing image sensor chips attached to an interposer according to a first embodiment of the present ~~invention.~~ invention;

Please amend paragraph number [0025] as follows:

[0025] FIG. 10 is a sectional side view showing a layer of encapsulant formed on the interposer of FIG. ~~9.~~ 9;

Please amend paragraph number [0026] as follows:

[0026] FIG. 11 is a sectional side view of image sensor package assemblies according to the first embodiment of the present ~~invention.~~ invention;

Please amend paragraph number [0027] as follows:

[0027] FIGS. 12-15 are sectional side views of the formation of image sensor package assemblies according to a variant of a second embodiment of the present ~~invention.~~ invention;

Please amend paragraph number [0028] as follows:

[0028] FIGS. 16-17 are sectional side views of the formation of image sensor package assemblies according to another variant of the second embodiment of the present ~~invention.~~ invention;

Please amend paragraph number [0029] as follows:

[0029] FIGS. 18 and 19 are sectional side views of the formation of image sensor package assemblies according to a third embodiment of the present ~~invention~~. invention;

Please amend paragraph number [0030] as follows:

[0030] FIG. 20 is a sectional side view of a preformed leadless chip carrier used in a fourth embodiment of the present ~~invention~~. invention;

Please amend paragraph number [0031] as follows:

[0031] FIGS. 21A-21C show image sensor package subassemblies affixed to the leadless chip carrier in a variant of the fourth embodiment of the present ~~invention~~. invention; and

Please amend paragraph number [0038] as follows:

[0038] After backgrinding wafer 2 to the desired thickness, a dicing operation is carried out to separate image sensor chips 4 from wafer 2. In a first stage of the dicing operation shown in FIG. 6A, transparent cover 22 is cut along the edge of the pattern of adhesive material 24 surrounding the image sensitive area 12 of each image sensor chip 4. FIG. 6B, which is an enlarged cross section of wafer 2 taken along line 6B-6B in FIG. 6A, shows that the bond pads 14 of each image sensor chip 4 (FIG. 1A) are left exposed for receiving electrical connections, while image sensitive area 12 is sealed by the remaining portion of transparent cover 22 overlying adhesive material 24. Cutting of transparent cover 22 may be accomplished, by way of example, using a saw blade (not shown) having a width that is equal to the distance 28 between adjacent edges of adhesive material 24 surrounding each image sensitive area 12. In this manner, the entire portion of transparent cover 22 between adjacent image sensitive areas 12 may be removed by a single saw pass along a street 8. A narrower saw blade may also be used, with two saw passes being made to expose bond pads 14.

Please amend paragraph number [0039] as follows:

[0039] FIGS. 7A and 7B show an alternative to the first stage of the dicing operation where adhesive material 24 has been formed in a pattern covering bond pads ~~14~~ 14, as previously depicted in FIG. 4B. In FIG. 7A, transparent cover 22 is cut with a narrow saw blade (not shown) down the middle of street 8. An etching process is then carried out to remove the portions of transparent cover 22 and adhesive material 24 covering bond pads 14, as seen in FIG. 7B. Using this alternative process protects bond pads 14 and prevents the deposition of contaminants while cutting transparent cover 22.

Please amend paragraph number [0040] as follows:

[0040] In a second stage of the dicing operation shown in FIG. 8, wafer 2 is cut along streets 8 (FIG. 7A) of semiconductor material at the outer edges 6 of image sensors chips 4 for complete separation of wafer 2 into individual image sensor chips 4. Any conventional process for cutting wafer 2 may be used, such as with a dicing saw. FIG. 8 shows that each individual image sensor chip 4 includes an image sensitive area 12 sealed by a remaining portion of transparent cover 22, as well as bond pads 14 left exposed for later electrical connection.

Please amend paragraph number [0041] as follows:

[0041] In the next stage of package formation according to the first embodiment, FIG. 9 shows that each individual image sensor chip 4 is affixed to an interposer 30. Interposer 30 includes conductive pathways 32 extending from attachment pads 34 on a first surface 36 of interposer ~~30 to 30~~, to external connection points 38 on a second, opposing surface 40 of interposer 30. Image sensor chips 4 may be adhesively mounted to the first surface 36 of interposer 30 with an adhesive element comprising a layer of adhesive 42 such as an epoxy or by an adhesive-coated tape in a lamination process as known in the art. Wire bonds 44 are then formed to electrically connect the image sensor chip bond pads 14 with the attachment pads 34 of interposer 30. As can be seen in FIG. 9, the first embodiment of the present invention enables

the wire bonding process to be carried out while image sensitive area 12 is sealed under transparent cover 22.

Please amend paragraph number [0042] as follows:

[0042] FIG. 10 shows that after the wire bonding process is complete, a layer of encapsulant material 46 is formed over the first surface 36 of interposer 30 to cover wire bonds 44 and surround the edges of the portion of transparent cover 22 attached to each image sensor chip 4. Encapsulant material 46 may comprise any conventional compound known for use in encapsulating semiconductor chips that exhibits low moisture uptake and good dimensional stability. Encapsulant material 46 should also be selected to have a coefficient of thermal expansion (CTE) that is compatible with those of interposer 30 and image sensor chips 4. Examples of encapsulant material 46 contemplated for use in the present invention ~~include~~ include, but are not limited ~~to~~ to, thermoset or thermoplastic curable compounds such as silicon-filled polymers or liquid crystal polymers. The layer of encapsulant material 46 may be formed on interposer 30 by known transfer molding, pot molding or injection molding, by liquid dispensing, by photolithographic or stereolithographic deposition processes, or as otherwise known in the art.

Please amend paragraph number [0045] as follows:

[0045] Image sensor package assemblies 50 according to a second embodiment of the present invention are formed in a manner similar to that of the first embodiment, except image sensor chips 4 are not connected to the interposer attachment pads 34 using wire bonds 44. Instead, the image sensor chips 4 are formed to include backside conductive elements configured for direct connection to attachment pads 34.

Please amend paragraph number [0048] as follows:

[0048] In another variant of the second embodiment, image sensor package formation is carried out in the same manner as in the first embodiment up through the dicing ~~operation~~

operation, described with respect to FIGS. 6A-8. According to this variant of the second embodiment, FIG. 16 shows that after separating the image sensor chips 4 from wafer 2, a redistribution layer (RDL) may be provided on each image sensor chip 4 in the form of conductive traces 56 extending from bond pads 14 to the edge of the active surface 10 and down to backside 18. Conductive traces 56 of the RDL may be formed with conventional processes such as by depositing a metallic layer onto the surfaces of image sensor chips 4 by sputtering or chemical vapor deposition (CVD) and then masking and etching the metallic layer to form individual traces. Alternatively, conductive traces 56 may be formed as a TAB-type assembly of preformed traces carried on a polymer film which are bonded to bond pads 14 and adhesively affixed to an image sensor chip 4 to extend around sides thereof and down to backside 18.

Please amend paragraph number [0049] as follows:

[0049] FIG. 17 shows that once conductive traces 56 are formed, backside conductive elements such as conductive bumps 54 may be formed on conductive traces 56 and directly connected to the ~~interposer~~-attachment pads 34 of interposer 30, as in the first variant of the second embodiment. Formation of the layer of encapsulant material 46, addition of discrete conductive elements 48, and cutting into individual image sensor package assemblies 50 may then be carried out in the same manner as described in the first embodiment of the present invention.

Please amend paragraph number [0050] as follows:

[0050] A third embodiment of the present invention is shown in FIGS. 18 and 19. According to the third embodiment, transparent cover 22 is not attached to the image sensor chips 4 at the wafer level. Instead, wafer 2 is initially diced into individual image sensor chips 4, and image sensor chips 4 are affixed to interposer 30 with adhesive layer 42 in an uncovered condition, as seen in FIG. 18. Wire bonds 44 are then formed to electrically connect the image sensor chip bond pads 14 with the attachment pads 34 of interposer 30. FIG. 19 shows that individual transparent covers 22' are subsequently attached to each of the image sensor chips 4

with adhesive material 24. Because wire bonds 44 are formed prior to attaching individual transparent covers 22', adhesive material 24 may be placed directly over the attachment point of wire bonds 44 and bond pads 14, thereby sealing the entire active surface 10 of an image sensor chip 4 in the area surrounding image sensitive area 12. This arrangement also allows individual transparent covers 22' to cover the entirety of active surface 10, which provides protection during subsequent processing. Formation of the layer of encapsulant material 46, addition of discrete conductive elements 48, and cutting into individual image sensor package assemblies 50 may then be carried out in the same manner as described in the first embodiment of the present invention.

Please amend paragraph number [0051] as follows:

[0051] In a fourth embodiment of the present invention, image sensor package assemblies are formed by mounting individual image sensor chips within the cavity of a preformed semiconductor package housing such as a leadless chip carrier (LCC). This enables a completed image sensor package ~~assembly~~ assembly, according to the present ~~invention~~ invention, to be attached to a carrier substrate or other higher-level circuit assembly at an attachment location configured with a standard package footprint. FIG. 20 shows an exemplary preformed package housing comprising a LCC 58 for use with image sensor package assemblies according to the fourth embodiment of the present invention. LCC 58 includes a body 60 of ceramic, plastic, or other conventional LCC package materials, and a chip cavity 62. Conductive pathways 64 extend from attachment pads 66 within chip cavity 60 to solder pads 68 formed about the exterior perimeter of body 60.

Please amend paragraph number [0052] as follows:

[0052] In one variant of the fourth embodiment, individual image sensor chips 4 having transparent covers 22 or 22' are formed and affixed to interposer 30 as in the first through third embodiments. Discrete conductive elements 48 are likewise added to the external connection points 38 of interposer 30. Rather than forming a layer of encapsulant material 46 on interposer

~~30 as 30, as~~ in the first through third embodiments, ~~however,~~ interposer 30 is singulated to form a packaging subassembly, which is mounted within chip cavity 62 of LCC 58 by bonding discrete conductive elements 48 to attachment pads 66, as seen in FIGS. 21A-21C. FIG. 21A shows a packaging subassembly 70 mounted within chip cavity 62, wherein image sensor chip 4 and transparent cover 22 have been formed and affixed to interposer 30 as in the first embodiment. FIG. 21B shows a packaging subassembly 72 mounted within chip cavity 62, wherein image sensor chip 4 and transparent cover 22 have been formed and affixed to interposer 30 as in the second embodiment. FIG. 21C shows a packaging subassembly 74 mounted within chip cavity 62, wherein image sensor chip 4 and individual transparent cover 22' have been formed and affixed to interposer 30 as in the third embodiment. FIGS. 21A-21C show that to complete the image sensor chip package assembly 50, chip cavity 62 is then filled with a liquid sealant 76 that covers the ~~packaging-subassembly-~~ subassemblies 70, 72, or 74 and surrounds the edges of the ~~transparent-cover-~~ covers 22 or 22' attached to each image sensor chip 4. Liquid sealant 76 may be a curable polymer compound, such as an epoxy, resin or molding compound, or any other liquid sealant material known for use in sealing semiconductor packaging.

Please amend paragraph number [0053] as follows:

[0053] Another variant of the fourth embodiment is shown in FIGS. 22A-22C. Under this approach, individual image sensor chips 4 are formed with transparent covers 22 or 22' as in the first through third embodiments, but are not affixed to interposer 30. Instead, they are affixed directly to the bottom of the LCC 58 chip cavity 62 and electrically connected to attachment pads 66 such that LCC 58 itself provides the interposer substrate, as seen in FIGS. 22A-22C. FIG. 22A shows that an image sensor chip 4 with transparent cover ~~22-~~ 22, attached as in the first ~~embodiment-~~ embodiment, is affixed to the bottom of chip cavity 62 with adhesive layer 42 and wire bonds 44 formed between bond pads 14 and attachment pads 66. FIG. 22B shows that an image sensor chip 4 with transparent cover ~~22-~~ 22, attached as in the second ~~embodiment~~ embodiment, is affixed to the bottom of chip cavity 62 by bonding backside conductive elements such as conductive bumps 54 directly to attachment pads 66. FIG. 22C shows that an image

sensor chip 4 with individual transparent cover-~~22'~~ 22', attached as in the third-embodiment embodiment, is affixed to the bottom of chip cavity 62 with adhesive layer 42 and wire bonds 44 formed between bond pads 14 and attachment pads 66. FIGS. 22A-22C show that to complete the image sensor chip package assembly 50, chip cavity 62 is then filled with liquid sealant 76 to cover image sensor chips 4 and surround the edges of the transparent-~~cover~~ covers 22 or 22'.